Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method comprising:

receiving a packet add (PADD) instruction comprising a result register identifier to identify a result register, a first source register identifier to identify a first source register storing a first operand, ~~and~~ an operand identifier to identify a second operand, and a carry in parameter to cause a dedicated PADD logic device to perform a packet addition of said first and second operands with a carry in to generate a result; and

in response to receiving said PADD instruction, causing ~~said~~a dedicated PADD logic device to perform a packet addition of the first and second operands to generate ~~the~~a result, and to subsequently store the result in said result register.

2. (Original) The method of claim 1, wherein said operand identifier identifies a second source register storing said second operand.

3. (Original) The method of claim 1, wherein said operand identifier identifies an immediate value to use as said second operand.

4. (Currently Amended) The method of claim 1, wherein said PADD instruction further comprises a start identifier to identify ~~the~~ a start bit of said first operand.

5. (Currently Amended) The method of claim 1, wherein said PADD instruction further comprises a stop identifier to identify ~~the~~ a stop bit of said first operand.

6. (Cancelled).

7. (Original) The method of claim 1, wherein said PADD instruction includes a data field parameter to indicate that only certain bits of the content stored in said first register serves as said first operand.

8. (Original) The method of claim 1, wherein said PADD instruction includes an immediate value parameter to indicate that an immediate value serves as said second operand.

9. (Currently Amended) An apparatus comprising:

a result register;

a first source register;

an instruction control device to receive a packet add (PADD) instruction comprising a result register identifier to identify said result register, a first source register identifier to identify said first source register storing a first operand, ~~and~~ an operand identifier to identify a second operand and a carry in parameter to cause a dedicated PADD logic device to perform a packet addition of said first and second operands with a carry in to generate said result; and

said [[a]] dedicated PADD logic device responsive to said instruction control device to perform a packet addition of the first and second operands with said carry in to generate a result subsequently stored in said result register.

10. (Original) The apparatus of claim 9, further comprising a second source register, wherein said operand identifier identifies said second source register as storing said second operand.

11. (Original) The apparatus of claim 9, wherein said operand identifier identifies an immediate value to use as said second operand.

12. (Currently Amended) The apparatus of claim 9, wherein said PADD instruction further comprises a start identifier to identify ~~the~~ a start bit of said first operand.

13. (Currently Amended) The apparatus of claim 9, wherein said PADD instruction further comprises a stop identifier to identify ~~the~~ a stop bit of said first operand.

14. (Cancelled).

15. (Original) The apparatus of claim 9, wherein said PADD instruction includes a data field parameter to indicate that only certain bits of the content stored in said first register serves as said first operand.

16. (Original) The apparatus of claim 9, wherein said PADD instruction includes an immediate value parameter to indicate that an immediate value serves as said second operand.

17-54. (Cancelled).

55. (New) A method comprising:

receiving a packet add (PADD) instruction comprising a result register identifier to identify a result register, a first source register identifier to identify a first source register storing a first operand, an operand identifier to identify a second operand, and a carry in parameter to cause packet addition of said first and second operands with a carry in; and

causing a logic device, upon receiving said PADD instruction, to perform a packet addition of said first and second operands with said carry in to generate a result, and to subsequently store the result in said result register.

56. (New) The method of claim 55, wherein said operand identifier identifies a second source register storing said second operand.

57. (New) The method of claim 55, wherein said operand identifier identifies an immediate value to use as said second operand.

58. (New) The method of claim 55, wherein said PADD instruction further comprises a start identifier to identify a start bit of said first operand.

59. (New) The method of claim 55, wherein said PADD instruction further comprises a stop identifier to identify a stop bit of said first operand.

60. (New) The method of claim 55, wherein said PADD instruction includes a data field parameter to indicate that only certain bits of the content stored in said first register serves as said first operand.

61. (New) The method of claim 55, wherein said PADD instruction includes an immediate value parameter to indicate that an immediate value serves as said second operand.